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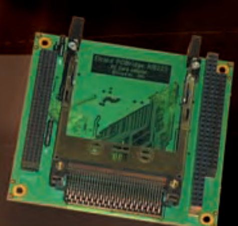

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Net-centric warfare: How embedded tech collides with the digitized battlefield, Halo, and the Internet
Nov. 12th • 2 p.m. EDT
Presented by: Curtiss-Wright, Mercury Computer Systems, AdvancedIO Systems, TEK Microsystems

Multicore: A look from three sides
Nov. 13, 2008 • 2 p.m. EDT
Presented by: Emerson Network Power, Freescale Semiconductor, and Wind River

ON THE COVER:
The USMC's Expeditionary Fighting Vehicle (originally the AAAV) is designed to exceed 25 knots in the water with its gas turbine engine, and can drive up onto the beach to penetrate deep into enemy territory at 45 mph. With its advanced weapons, C4ISR capability, and connection to the GIG, it's loaded with hot electronics. The Command Variant of the EFV uses a closed-loop liquid spray cooling system to keep COTS assemblies cool. See article on page 26. (Photo courtesy of U.S. Marine Corps)

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By Andy Anderson, AtHoc

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Image fusion enhances light armored vehicle capability

By Duncan Young

There is a wide variety of video imaging sensors, each offering optimal viewing or detection characteristics depending on the type of object being observed and the meteorological, lighting, or background conditions. To maximize the probability of detection, images from more than one sensor can be compared in real time to maintain image context and highlight objects of interest. Images can be displayed from each sensor side-by-side for an operator to discriminate directly. Or, alternatively, the images can be fused to create a truly realistic composite view from both sensors. Such a sensor fusion system would be ideal for deployment on light armored vehicles or Unmanned Aerial Vehicles (UAVs) if the critical criteria of space, weight, power, and affordability are met.

A typical small armored vehicle will often be fitted with two or more cameras, each operating in different parts of the spectrum (for example, visible, near infrared, or thermal infrared). In general, a thermal imager is best at detecting the thermal signature of troops or ground vehicles. In contrast, the background – and therefore, the context for the objects – can be identified better from the visible image. The context contains important information enabling a reconnaissance mission to report accurate dispositions of hostile troops or vehicles to other participants, for example (Figure 1).

The figure's leftmost image is from a TV camera, and the center image is from a thermal infrared camera that cannot discriminate the background detail because of adverse weather conditions. The fused image on the right clearly shows both the vehicle (which has been reversed to black) and the background detail together. Using information in this way has great practical advantages for tactical or covert surveillance as multiple sensors can see through smoke, mist, precipitation, and camouflage. When used from the air, image fusion provides better definition of topographical features, while the visible spectrum also provides color discrimination between similar object types.

Fusion techniques

One method for fusing images is to use linear combination of pixel intensity. However, this relies on matched optical characteristics of the sensors. It also has the effect of highlighting or even canceling objects that appear on both sensors while dimming those that appear on only one. An alternative technique is to use colors to differentiate between the images, but this results in a loss of realism. The final alternative, which avoids these unwanted effects, is to use a multiresolution algorithm. It decomposes each of the images into low, medium, and high resolutions to provide spatial, sized, and detailed representations that are then combined with different weightings to form the displayable image. The algorithm preserves the clarity of objects detected by only one sensor and combines objects from both sensors in a natural form.

Whichever method is used to fuse the images, additional correction is required to resolve physical and temporal misalignment. Physical misalignment can be caused by the positions of the sensors on the vehicle or by unmatched optical characteristics. This can be corrected by warping one image to fit the other. Temporal alignment is often required if the sensors or their video transmission paths delay one image stream more than the other, resulting in moving objects appearing in more than one position.

Hardware or software solution

Image fusion could be implemented just in software, particularly where raw sensor images can be packetized and streamed over a network to centralized computing resources. However, this level of resource is unusual for small, light armored vehicles, making a hardware solution an attractive alternative. To meet this demand, GE Fanuc Intelligent Platforms has developed the IMP20 image fusion module, measuring only 4" x 2.7" x 0.5" (100 mm x 68 mm x 12 mm). It accepts PAL or NTSC video from two out of three sources. Using a new approach to the multiresolution algorithm, it performs image fusion and image warping in real time. Accordingly, it provides a video output that can be synchronized to a central source and overlaid with graphical symbology if required.

Image fusion is now a practical and affordable technology for a broad range of light tactical ground vehicles and other sensor platforms. It can be deployed with no additional embedded computing support to provide enhanced detection capability. Combined with other image processing technologies such as tracking and recognition/classification, it can provide the "extra edge" critical to battlefield situational awareness.

To learn more, e-mail Duncan Young at young.duncan1@btinternet.com.

Figure 1

Enhanced network security protects war-fighters' platforms

By John Wemekamp

The rollout of planned Network Enabled Capability (NEC) by a number of nations' armed forces highlights the need for renewed emphasis on security. Networks are being implemented that encompass all levels of information and intelligence exchange from strategic planning, logistics, battle groups, and sensor and weapons platforms down to the tactical deployment of individuals. These networks will support not just national interests, but will also be required to support interoperability between allies and coalition partners with all the attendant issues of language, politics, culture, dissimilar assets, and doctrine. IPv6 has been selected as a secure backbone for the U.S. Global Information Grid (GIG), yet many more measures will be required to provide network integrity, data protection, and intelligence security in order to prevent attack or unauthorized access.

At the higher layers it is the responsibility of an application, its administrators, and users to maintain security. Applications are designed to prevent unauthorized user access and constantly monitor for malicious interference from insiders or disgruntled users. Shared applications over the Internet can make use of Transport Layer Security (TLS) or the earlier Secure Sockets Layer (SSL) to provide security within the application itself. These methods use authentication, keys, and encryption negotiated between servers and authorized clients.

Secure IP communications

Of course, it is at the application level that issues of culture, language, and doctrine are addressed. Similarly, TLS and SSL implementations are often specific to each type of application, putting them beyond the scope of the typical COTS vendor's product portfolio. However, IP has demonstrated vulnerabilities to a number of different attack types at routers, switches, and servers. Consequently, this is where COTS vendors' products can be used to advantage, introducing defensive technologies to protect sensitive network assets. The most common forms of attack are sniffing, planting, connection hijacking, and Denial of Service (DoS). *Sniffing,* or eavesdropping, happens when the unprotected packet payload can be read by an intruder without the communicating nodes' knowledge. *Planting* uses a similar technique to replace the payload with either modified data or malicious code such as a *Trojan Horse*. *Connection hijacking* occurs when an attacker is able to spoof a node into believing it is connected to a legitimate network node. Hijacking can be further developed to *DoS,* where the hijacked node is, for example, a server connection that is then bombarded with access requests. These swamp the server and prevent access by legitimate clients.

"The sheer size of the existing installed IPv4 base currently without IPsec, coupled with the diversity of developing national NEC efforts, exposes vulnerabilities to attack at the IP level."

IPsec was developed to address many of these vulnerabilities. IPsec introduces authentication, keywords, and encryption to the network layer, independent of any applications running on the network. It is equally applicable to IPv4 and IPv6, though its use is only mandated for IPv6. IPsec imposes additional processing overhead for authentication and encryption/decryption of the packet payload, often requiring retrospective upgrading of existing IPv4 equipment to be fully IPsec compliant. The sheer size of the existing installed IPv4 base currently without IPsec, coupled with the diversity of developing national NEC efforts, exposes vulnerabilities to attack at the IP level.

Intra-platform network security

Secure Virtual Private Networks (VPNs) such as intra-platform networks on armored vehicles, Unmanned Aerial Vehicles (UAVs), aircraft, and naval vessels require strong perimeter defense if they are to provide a safe and secure backbone network. At the same, time these platforms will be participating in shared applications as part of the networked battlefield and provide broader network access for communications, interoperability with partners, logistics, and support. Access protection from threats to IP integrity can be enhanced by the addition of a stateful firewall, IPsec/L2TP secure tunneling support, Network Address Translation (NAT) routing to detect IPv4 addressing irregularities, and intrusion filtering. The PMC-110 CryptoNet module from Curtiss-Wright Controls Embedded Computing (CWCEC) shown in Figure 1 is an example of such an enhanced security module, designed to complement an embedded switch or router to secure a VPN.

Figure 1

IPsec provides the basis of a secure environment for IP communications, though it will be many years before it can be implemented universally. Many new intra-platform networks can be implemented entirely in IPv6, as mandated by the DoD, using COTS equipment; however, they will inevitably be exposed in order to participate in the broader NEC and Internet environments. Until network layer communication is considered safe, adding further protection at vulnerable points is the most practical and affordable solution to enhanced network security.

To learn more, e-mail John at john.wemekamp@curtisswright.com.

Daily Briefing: News Snippets

By Sharon Schnakenburg, Associate Editor

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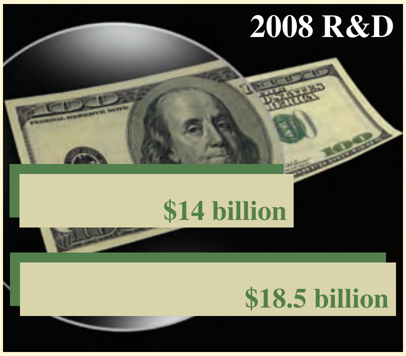
SIA, ITAA applaud U.S. '$700 billion bailout'



Amidst the controversy surrounding the "$700 billion bailout" or "Emergency Economic Stabilization Act" recently signed into U.S. law, the Semiconductor Industry Association (SIA) and the Information Technology Association of America (ITAA) have released statements voicing their approval. "We applaud the President and members of the Senate and House of Representatives for … enactment of the financial services rescue measure," George Scalise, SIA president, says. "We are also very pleased that the bill includes a two-year R&D tax credit extension." SIA estimates that more than 50,000 of 216,000 U.S. semiconductor industry employees work in R&D. Meanwhile, ITAA estimates some $14 billion in R&D opportunities were likely lost in the interim. "The R&D credit would have spurred more than $18.594 billion in new economic activity in [all of] 2008. Those economic gains were put at risk during the nearly 10 months the credit was lapsed," says Charles Greenwald, ITAA representative. The new R&D tax credit extension is retroactive from Jan. 1, 2008 and runs through Dec. 31, 2009.

USMC: Knowledge is key

Awareness is often the first step, a mantra the U.S. Marine Corps is taking to task. Case in point: The USMC recently issued a delivery order for $23.2 million to L-3 Communications to provide 600 of its mobile VideoScout-MC video exploitation, acquisition, and management systems. The VideoScout-MC laptop computers, which feature integrated multiband receivers, will provide real-time video imagery for increased battlefield situational awareness. Metadata and video are captured from Unmanned Aerial Systems (UASs), intelligence feeds, targeting PODs, and other sensors, and are indexed and stored automatically. They can also be viewed, annotated, archived, or geo-referenced, then sent to other personnel. Delivery is expected in Q408.

NATO gets help with heavy lifting

A consortium consisting of 10 NATO members and 2 Partnership for Peace countries has reached an understanding – or rather signed a Memorandum of Understanding (MOU) – to acquire three Boeing C-17 Globemaster III aircraft. The multinational consortium's agreement with the NATO Airlift Management Agency and the U.S. DoD is part of NATO's Strategic Airlift Capability (SAC) program, slated to provide advanced airlift capabilities in Afghanistan and on U.N. and E.U. missions. The MOU stipulates that one C-17 is provided by the U.S. Air Force, the other two by Boeing. The C-17 long-range cargo jets will be stationed at Papa Air Force Base in Hungary and operated jointly by all 12 consortium nations: Hungary, Lithuania, Norway, The Netherlands, Poland, Bulgaria, Slovenia, Estonia, Romania, the United States, Sweden, and Finland. Each country will pay for only part of the C-17 instead of a whole aircraft, and the first C-17 delivery could occur by spring 2009. The MOU represents the first major NATO defense acquisition in three decades, Boeing reports.

U.S. Air Force photo by Airman 1st Class Tony Ritter

Northrop Grumman is right on target

Northrop Grumman will soon prove that precision is key on the battlefield: Its LRS-2000 Rate Sensor Assembly (RSA), boasting a drift rate under one degree per hour, was recently chosen by prime General Dynamics Land Systems to be part of the U.S. Army's Stabilized Commander's Weapon Station (SCWS) for the M1A1 Abrams tank. SCWS offers increased protection from IEDs and enemy gunfire by enabling soldiers to stay inside the tank while firing the M1A1's machine gun. Meanwhile, the LRS-2000 RSA features a two-axis design and supports targeting applications. LRS-2000 RSA is based on Northrop Grumman's dynamically tuned G-2000 gyro, which provides an MTBF of more than 100,000 hours. The LRS-2000 RSA prototype passed Army field testing in July, and the first production unit delivery is expected in June 2009.

TECOM to become more secure

Insecurity is generally deemed a negative trait, and experts agree it is particularly harmful in high tech, in light of external security attacks. Thus, the Information Technology for European Advancement (ITEA) consortium recently signed on mission- and safety-critical software solutions provider Aonix for the Trusted Embedded COMputing (TECOM) project. TECOM aims to develop an execution environment that is secure enough to withstand such attacks. Aonix will lend both its security expertise and an adapted version of its (Java) PERC Ultra virtual machine to TECOM. The adapted PERC will include integration with TECOM trusted OSs and the TECOM middleware security layer. Additionally, it will provide a partitioned execution environment within multi-application systems.

EADS eases transition to U.S. locale

While transitions are typically accompanied by obstacles, EADS North America reports that its plan to gradually and fully transition production of the U.S. Army's UH-72A Lakota Light Utility Helicopter to U.S. soil is progressing smoothly. Accordingly, the company recently delivered the first Final Assembly Line (FAL) version of the UH-72A to the Army from EADS' Columbus, Mississippi Eurocopter facility. The company was awarded the UH-72A contract in 2006, and continues to transition toward full U.S. production in three phases: Light Assembly Line (LAL), FAL, and Production Line (PL). The FAL helicopter finished 7 of 14 production assembly stations in the U.S. and is EADS North America's 41st UH-72A delivery. No. 41 also includes the first tail boom manufactured entirely in the U.S. The Lakotas will continue in the FAL phase until they can move through all 14 Columbus stations, signifying full U.S. production transition. UH-72As are anticipated for use in homeland security, Army National Guard and Army logistics, and MEDEVAC operations.

U.S. Army photo by Pfc. Coltin Heller

Continued on page 14

 Continued from page 13

USJFCOM revamps contract recompete

To invoke a win/win situation for companies both large and small, war fighters, and even taxpayers, the U.S. Joint Forces Command (USJFCOM) recently announced it will change its Joint Concept Development and Experimentation Directorate (J9) contract's composition. Expiring in summer 2009, the $478 million contract's recompetition will include multiple contracts instead of only one large contract, in an effort to foster competition, lower prices, and improve project manageability and access to talent. The recompetition began in October, with anticipation of in-place solicitations by 2008's year end. This new recompete approach is in lockstep with the 2008 National Defense Authorization Act to reduce single-award contracts of large magnitude, USJFCOM reports.

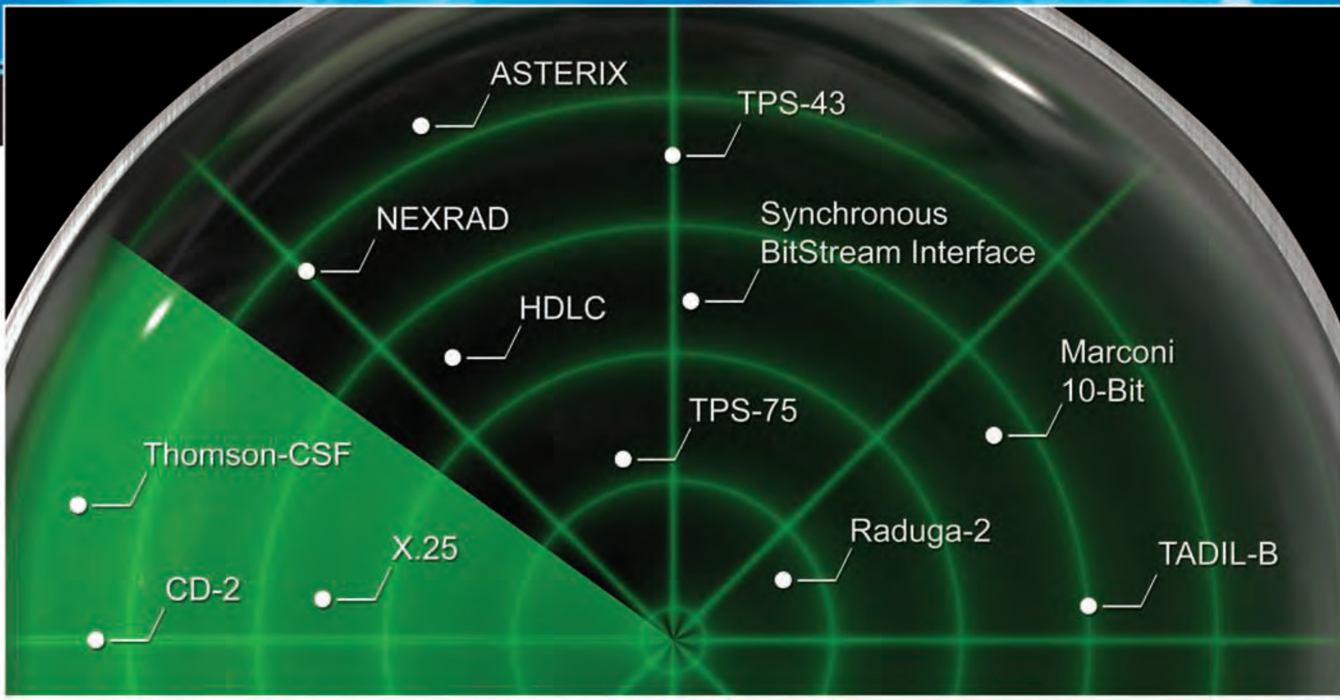
'Obsolescence-proof design' now available

Some things never go out of style. At least that's what Quantum3D is banking on with the claim that its Sentiris AV1 XMC features an "obsolescence-proof design." Their assertion is founded on the XMC's utilization of a Xilinx Virtex-5 FPGA-based graphics- and video-processing core instead of traditional dedicated Graphics Processing Units (GPUs). GPUs can rapidly go obsolete via End-of-Life (EOL) notices, the company says; however, the FPGA is programmed like an embedded GPU and is upgradeable over the product's lifetime. In addition, the Sentiris AV1 XMC includes fully DO-254 certifiable firmware and can be integrated with any CPU environment or OS. The conduction-cooled XMC meets MIL-STD-810F for harsh environments. It also offers 512 MB ECC-protected DDR2 memory, eight PCI Express lanes, dual HD-SDI outputs, and dual RGB.

Water, water everywhere … yet nowhere

As scientists ponder the mystery of where the Red Planet's once-liquid water disappeared to, Lockheed Martin and NASA will conduct definitive research via NASA's Mars Atmosphere and Volatile EvolutioN (MAVEN) program to find the answer. The $485 million project analyzes Mars' past weather changes and upper atmosphere, and is led by the University of Colorado's Laboratory for Atmospheric and Space Physics (LASP). Planned for a late 2013 launch and fall 2015 Mars landing, MAVEN focuses on the role of solar wind and its contribution to current atmospheric losses. MAVEN is based on the designs of Lockheed Martin's 2001 Mars Odyssey spacecraft and Mars Reconnaissance Orbiter (MRO), both of which are still orbiting Mars and conducting scientific operations. MAVEN is NASA's Mars Scout Program's second mission, while the Phoenix Mars Lander is the first.

Artist's rendition courtesy of NASA



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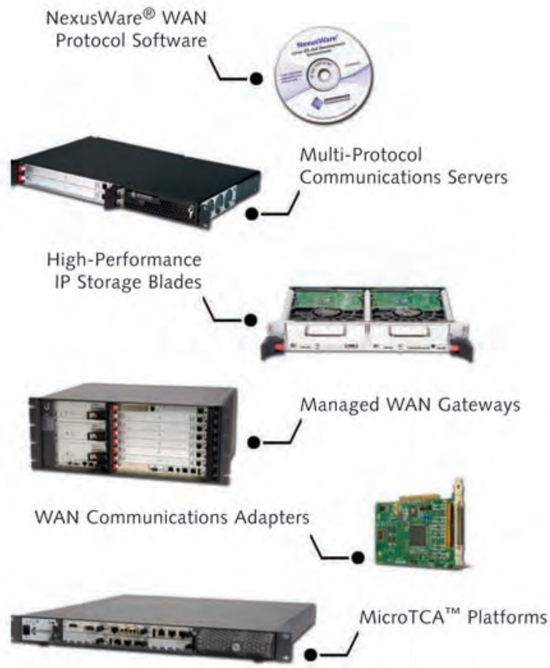

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U.S. Air Force photo by Airman 1st Class Jonathan Snyder

Flexible, data-centric UAV platform eases mission adaptation

By Edwin de Jong, Ph.D.

Because Unmanned Air Vehicles (UAVs) are invariably designed for specific missions, they tend to be difficult to adapt to changes in mission once built and deployed. Building a UAV that is readily adaptable to different mission parameters requires a new platform approach to UAV architecture. The biggest advantages are significant savings in cost, complexity, and time in the operational phase. Part of the technical challenge in building a UAV platform is providing an integration framework that supports this approach. Such an integration framework can be implemented through the use of middleware to abstract the details of point-to-point data transmission away from the individual components of the UAV. This type of middleware has been created as the Data Distribution Service for Real-Time Systems (DDS), a standard published by the Object Management Group (OMG) and currently used in implementations of both UAVs and ground stations.

The growing drive to employ UAVs for a variety of defense and commercial purposes has exposed weaknesses and limitations of traditional design strategies. Because UAVs were invariably designed for specific missions, they tend to be difficult to adapt to changes in mission once built and deployed. A new set of mission profiles necessitates the design of yet another UAV. Consequently, over time, manufacturers and user organizations have to maintain production and support lines for multiple UAV systems, all having a common architecture but needing different performance, connectivity, or data characteristics.

Ideally, two or three UAV designs could serve as platforms that could be readily adapted to a variety of different missions. The platforms would be differentiated by their physical characteristics, such as power plant, airframe, and fuel capacity, with complementary hardware and software. For mission flexibility, components should be field replaceable and hot swappable on the platform without disruption. The software infrastructure should provide automatic discovery and configuration, so that components can be added and removed dynamically on a live system and immediately recognized and integrated with the system. Also, nodes should be able to restart after failure at any time, and applications should be able to start in any order.

Conceptually this idea is easy to understand, but technically it cannot be easily implemented using current design principles. Today, each vehicle design requires a special-purpose ground station, which is well integrated but expensive. UAV flight software is typically redesigned for each new vehicle, and even sometimes for different missions or payloads on the same vehicle. Building a UAV that is readily adaptable to different mission parameters doesn't seem feasible.

Rather, it requires a new architecture for systems design and implementation – one that provides both the features and the flexibility to take on multiple roles and missions without returning to the drawing board for substantial modifications. Consider this the "platform approach" to UAV design. By itself, the UAV platform isn't a specialist in any single mission profile. When configured with the appropriate hardware and software, a small number of UAV platforms might be able to serve a wide variety of different missions effectively, and DDS middleware is key to this multi-mission framework.

Configurable UAV platforms reduce complexity

The success of a configurable UAV platform in fulfilling multiple missions has the potential to affect the entire UAV product life cycle. Design and implementation are likely to be less complex, as the platform is conceptually and technically simpler. Design parameters will change, because of the need to support a larger range of missions, but should become less complex overall.

The biggest advantages are likely to be seen in the operational phase of the life cycle. First, there will be fewer UAV models to support – perhaps two or three platforms rather than a dozen or more different models. This makes provisioning simpler and less expensive, and inventory management becomes less complex. But ultimately it reduces support complexity and costs, because one ground station can serve the platform, rather than requiring separate ground configurations for each separate UAV model. Since the UAV platform by itself is not equipped for any specific mission profile, it is likely that more components and technical support will be required to reconfigure UAV platforms into specific roles and missions. This, however, will be more than offset by the advantages gained in supporting and provisioning fewer UAV models and designing and implementing architecturally simpler UAV platforms.

Integration framework connectivity solves challenge

Getting to the point where a UAV design can serve as a multi-mission platform is a significant technical challenge. A large part of that challenge is providing an integration framework that supports that concept. Today, UAV implementation is driven by dedicated, hardwired connections between instruments, data collection devices, control surfaces, and the ground control station. While this configuration can guarantee data availability across the components that require data for real-time response, it becomes complex when there are more than a handful of interconnections.

Further, a hardwired configuration is highly resistant to change. For example, if bandwidth requirements were to increase in the future because of new instruments, subsystems, or sensors, it might not be possible to obtain the needed performance or availability guarantees on that UAV. In fact, that is one of the reasons why UAVs tend to be mission-specific.

Conversely, a true platform accommodates full interconnectivity between all possible data sources and consumers. At first glance, that can be enormously complex because there are no preconceived notions of data paths, network bandwidth, or time determinism. Even if such a configuration could be designed and built, there seemingly could be no guarantee that the available bandwidth would meet the actual performance and real-time requirements of any given combination of instruments.

A platform also requires the ability to deliver the necessary bandwidth, performance, and guarantees to any possible configuration. Of course, there are always cases that demand trade-offs in order to achieve this, but the technical trade-offs between performance, reliability, and real-time determinism, for instance, should be both possible and reasonable for the multi-mission integration framework.

Data-centric architecture via DDS

Such an integration framework can be implemented through the use of a software layer, or middleware, that abstracts the details of point-to-point data transmission away from the UAV's individual components. In doing so, this middleware can offer the ability to easily add new hardware and applications, make data available using multiple available routes to ensure real-time availability, support multiple transport protocols, and provide for tuning to specific configurations and missions.

This type of software layer has been created as the Data Distribution Service for Real-Time Systems, a standard published by the Object Management Group. The Data Distribution Service uses the publish-subscribe communications model to enable data producers to publish data to the infrastructure and allow data consumers to subscribe to data from this data infrastructure. The DDS publish-subscribe model automatically connects information producers (publishers) with information consumers (subscribers). The communications are decoupled in space (nodes can be anywhere), time (delivery may be immediately after publication or later), and flow (delivery may be made reliably, tuned to available bandwidth).

In a DDS implementation, the data is abstracted away from the physical source and destination and made accessible to any application that subscribes to it, independent of the source's location and the specific link technology that transports the data (Figure 1). Since DDS coupling is loose and anonymous, communication paths can be defined, created, and destroyed at runtime. Further, DDS implementations automatically "discover" requesting publishers and subscribers, establishing connection between them at runtime with no previous configuration. DDS also enables a resiliency of data necessary for fault tolerance across the network.

Additionally, in considering our multi-mission UAV platform, the DDS standard defines a comprehensive set of Quality of Service (QoS) parameters. Because there might be design trade-offs, engineers can configure a balance between performance, reliability, determinism, and other factors affecting the system's ability to perform its mission. DDS QoS parameters specify the degree of coupling between components and properties of the overall model and of the data transfers themselves.

DDS includes QoS parameters such as reliability, durability, deadline, priority, and data ownership. By adjusting QoS parameters, system and application software developers will be able to ensure that data transmission and reception meet the unique needs of each system and

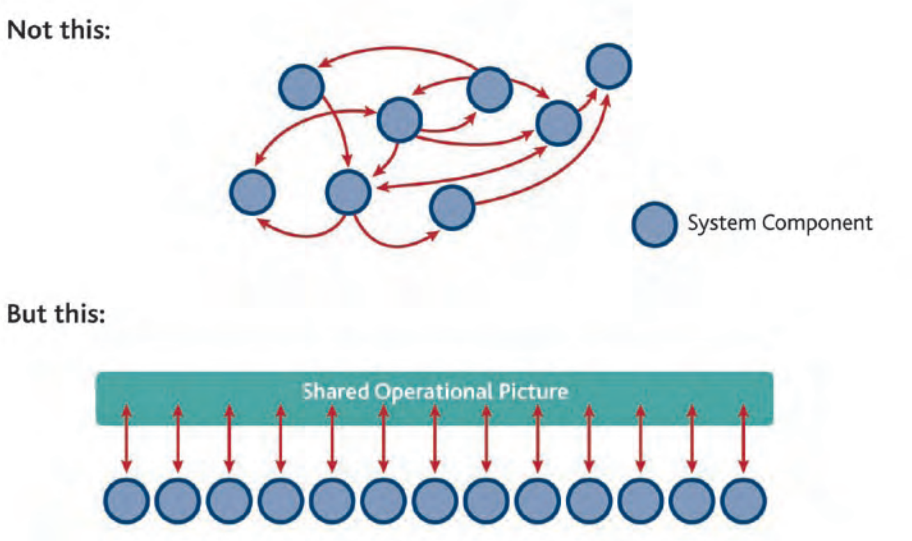

Figure 1

application. It is possible to change QoS parameter settings at runtime, supporting reconfiguration for a specific mission without the need to rebuild application software. The rich QoS parameter set makes it possible to implement DDS on a wide range of processors and networks, including those that are embedded.

DDS is fundamentally designed to work over unreliable transports, such as UDP or wireless networks. No facilities require central servers or special nodes. All communication, including discovery, is strictly peer-to-peer and optionally employs multicasting for efficiency and scalability.

Example: A data-centric integration foundation

Consider a UAV that has been designed with a DDS implementation serving as a software integration platform supporting largely interchangeable hardware and applications. Implementing DDS middleware as the foundation for data communication affords a great deal of flexibility on the actual payload. It can focus on sensors and data recording instruments, ensuring that continuous data streams are available to record and analyze data. Or it can focus on real-time communication, ensuring that telemetry data to and from the ground station is exchanged reliably and deterministically. Once the platform has been created, engineers can look closely at QoS trade-offs to ensure that system data availability requirements are met. QoS settings can be changed at runtime to meet specific mission requirements.

Emerging uses in UAV design

DDS is currently used in implementations of both UAVs and ground stations. For example, DDS middleware underlies the General Atomics Advanced Cockpit Ground Control Station (GCS). The GCS networking system integrates controls and information displays, synthetic video, and fused situational awareness data.

The DDS middleware forms the software communications backbone of this station. The DDS publish-subscribe architecture eases system integration for communications. For instance, any system component can subscribe to the incoming aircraft telemetry stream, such as latitude and longitude, pitch, roll, and airspeed parameters. It also allows users to connect multiple workstations, for instance, allowing a pilot at one station to work closely with a sensor operator at a different station.

As another example, the Insitu ScanEagle long endurance UAV uses DDS on the vehicle itself and in the ground control stations (Figure 2). On the airframe, DDS connects the flight computers, sensors, and onboard application computers. Within the ground station, DDS connects the systems that decode data feeds, analyze the UAV's situation, and interface to the operator control. DDS implements a hierarchical control network with well-controlled data flows. This allows Insitu, for instance, to seamlessly switch control between multiple ground stations and to reliably connect to the aircraft over unreliable low-bandwidth links.

The DDS QoS configurability also makes it well suited to lossy networks such as might be encountered with the wireless connections between the vehicle and ground station.

Of course, DDS doesn't address all of the challenges surrounding the implementation of a flexible UAV platform. Factors such as equipment and payload weight,

Figure 2

aerodynamic balance, cost, and power consumption will drive different UAV platforms, even with a flexible and responsive integration model. But given the capabilities of the DDS standard for abstracting and managing real-time data flow, it can offer a fundamental approach to building a multi-purpose UAV platform.

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The Defense Electronic Product Source

Nov/Dec 2008

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The 5000 Series of surface-mount common mode chokes provides line filtering for designers of power converters looking to reduce unwanted common mode noise in EMC-sensitive applications. The chokes' inductance values range from 0.47 mH to 4.7 mH, and the series features a DC current rating of up to 700 mA. The chokes can attenuate at frequencies of up to 100 MHz and are suited for use in low-current DC input switching power supplies. Measuring 7.0 mm x 5.9 mm x 4.4 mm with an industry-standard pad layout, all choke package materials are UL94 V-0 rated. Additionally, the devices are RoHS and JEDEC J-STD-020-C reflow compliant. Operating temperature ranges from -40 °C to +85 °C.

www.murata-ps.com

MURATA POWER SOLUTIONS

Ultra-miniature DC/DC converters

The RP-15SAW is a 15 W power package combining ultra-miniature dimensions with ultra-wide input voltage ranges. RP-15SAW measures a miniscule 1" x 1" (25.4 mm x 25.4 mm) with a height of 0.39" (10 mm). High-efficiency grades up to 87 percent are a must for these galvanically isolated DC/DC converters, and guarantee trouble-free operation at ambient temperatures exceeding 60 °C without external cooling measures. (Packing density reaches 2.3 W/cm^3). The outputs are trimmable in the range of ±10 percent of nominal output voltage. Meanwhile, electrical specifications include 2:1 inputs of 9 to 18 V, 18 to 36 V, and 36 to 75 V as well as 4:1 input ranges of 9 to 36 V and 18 to 75 V. Output voltages are set at 3.3 V, 5 V, 12 V, and 15 V. The output rating is 15 W, and the isolation voltage is 1,600 VDC. Vacuum potting qualifies these converters for the most stringent temperature and vibration conditions.

www.recom-international.com

RECOM POWER LABORATORY

Compact 150 W power supply

The P140R is a compact 150 W power supply available in four versions with 5 V, 12 to 15 V, 24 V, and 48 V DC output. Designed for hot-swap (N+1 redundancy), the P140R employs a "smart" load share. This thermal load share automatically pools all paralleled power supplies and splits the load current so that all power supplies are kept at roughly the same temperature level. To manage the internal functions of these new power supplies, microcontrollers are used. In addition to multivoltage input ranging from 85 V AC to 264 V AC, the power supply features active Power Factor Correction (PFC) and a synchronized rectifier. It is also equipped with protective measures against overvoltage, overload, and excess temperature. The typical H15-type connector (EN 60603) provides full compatibility with the industry standard. Operating temperature ranges from -25 °C to +70 °C, and PR140R uses a Euroboard that allows easy integration into 19" systems.

www.mgv.de

MGV STROMVERSORGUNGEN

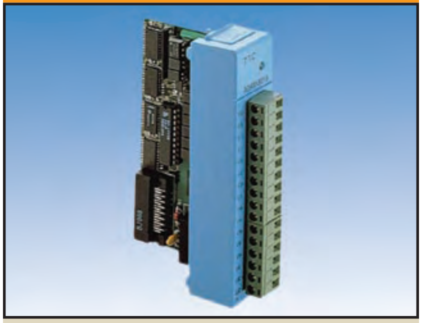
Frequency and phase converter

The ED-FPC is a lightweight frequency and phase converter providing reliable computer-grade power for use in aircraft, ground-based, and mobile systems such as an HMMWV. Therefore, it is designed to meet the shock and vibration requirements of RTCA/DO160, Zone A, and the Munson Road test. The rack-mount converter ranges from 3 to 5 kVA and weighs less than 80 pounds in a compact 7" (4U) high form factor. It includes a three-phase input accepting a 45-450 Hz input frequency range. Having a single-phase 120 VAC, 50, 60, or 400 Hz output, the ED-FPC eliminates phase imbalance problems associated with powering large single-phase equipment from a three-phase generator source. It also eliminates line-side voltage transients, surges, sags, and frequency stability problems. Additionally, it provides a superior low-distortion sinewave output with ±3 percent voltage regulation.

www.falconups.com

FALCON ELECTRIC, INC.

Thermocouple input module



The ADAM-5018 is a seven-channel thermocouple input module that features programmable input ranges on all channels. It accepts millivolt inputs (±15 mV, ±50 mV, ±100 mV, ±500 mV), voltage inputs (±1 V, ±2.5 V), current input (±20 mA, requires 125 ohms resistor), and thermocouple inputs (J, K, T, R, S, E, B). The module forwards the data to the host computer in engineering units (mV, V, mA, or temperature °C). Isolation voltage is 3,000 VDC, and effective resolution is 16 bit. ADAM-5018 provides a sampling rate of 10 samples/sec. (total), accuracy of ±0.1 percent or better, and withstands overvoltages up to ±35 V.

www.advantech.com
ADVANTECH

MIL/COTS attenuator module

The M-FIAM9 is a military COTS filter input attenuator module providing EMI filtering and transient protection. It enables designs to meet conducted emission/susceptibility per MIL-STD-461E and input transients per MIL-STD-704A/E/F and MIL-STD-1275A/B/D. M-FIAM9, which measures 2.28" x 2.2" x 0.5" (57.9 mm x 55.9 mm x 12.7 mm), accepts an input voltage of 10 to 36 VDC and delivers output power up to 500 W. Available in two environmental grades (-55 °C to +100 °C operating and -65 °C to +125 °C storage), M-FIAM9 includes four pin options and three baseplate options.

www.vicorpower.com
VICOR CORPORATION

High-power lithium battery

Tadiran's TLM 1550-HP is a high-power lithium battery currently employed in UAV applications. It is also suitable for rockets and missiles, smart ammunition, sonobuoys, listening devices, weapon sights, sensors for dispersed munitions, and tracing devices, among others. It utilizes COTS technology that is highly adaptable to application-specific requirements. AA-size batteries deliver 2 Watt/hours of energy with an open circuit voltage of 4.0 V, capable of handling pulses of up to 15 A and 5 A maximum continuous current at 3.2 V. Smaller cells, including sub-1/2AA and 2/3AA sizes, are also available. Cells provide up to 20 years of service life, and can be periodically tested without having to fully discharge the battery. Rugged and capable of withstanding extreme temperatures from -40 °C to +85 °C, they provide fast activation with instantaneous voltage after prolonged storage.

www.tadiranbat.com **TADIRAN**

COTS EMI filter module

The VPTF20-28 is a COTS EMI filter module in compliance with MIL-STD-461 C/D/E for conducted emissions in military and avionics DC-DC power systems. Specifically intended for use in harsh environments with extreme shock, vibration, and temperature cycling, the filters feature up to 20 A maximum current and up to 300 W output power. Wide input voltage range is 0 to 50 V per MIL-STD-704, with 28 V nominal. The module is manufactured to J-STD-001, ISO9001, and IPC-A-610 and operates over -55 °C to +100 °C. Inside a six-sided rugged metal enclosure, VPTF20-28 provides 45 dB minimum attenuation at 500 KHz. Meanwhile, its high input transient voltage is 80 V for 1 sec per MIL-STD-704A.

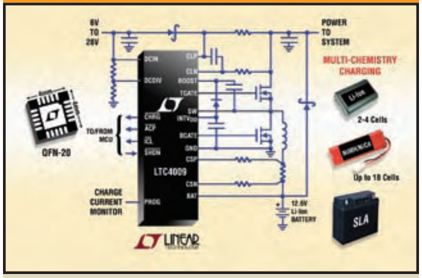
www.vpt-inc.com **VPT, INC.**

Output power monitor IC

The IR3720 is an output power monitor IC with digital I²C interface for low-voltage DC-DC converters used in notebook and desktop computers and energy-efficient server applications. It achieves current accuracy within 0.2 percent typical error over all input voltage and load ranges. The IC also provides 3.3 percent power accuracy, ±.75 percent voltage accuracy, +3.3 V ±5 percent bias supply voltage, and operates within -10 °C to +150 °C. The IR3720 measures dynamic power at the output or load side of the voltage regulator, and it monitors the output filter inductor current in buck or multiphase converters from 0.5 V to 1.8 V. Additionally, IR3720 gives designers the option to use resistive sensing or inductor DCR current sensing with an internal thermal compensation feature for high efficiency and reduced board size.

www.irf.com **INTERNATIONAL RECTIFIER**

Battery charger controller

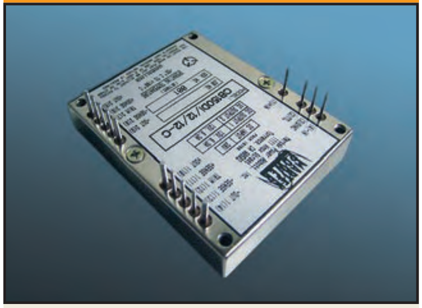


The LTC4009 is general-purpose battery charger controller featuring a 550 KHz synchronous buck PWM topology. It provides ±0.5 percent output voltage accuracy, 4 percent accuracy for programmable charge current, and 3 percent accuracy for programmable AC adapter current limit. Input voltage range is 6 V to 28 V, and output voltage range is 5 V to 28 V. LTC4009 includes an analog charge current monitor, micropower shutdown, and a thermally enhanced, 20-pin, 4 mm × 4 mm × 0.75 mm QFN package.

www.linear.com

LINEAR TECHNOLOGY CORPORATION

Dual output power supply



The CB150D is a 150 W dual-output DC-DC power supply. It is designed for applications in the military, industrial, and aerospace realms, and features two independent 75 W outputs ranging from 2 V to 28 V. Its input range is 16 to 40 VDC, and power density is 45 W/in^3. Other features include remote turn on/off (TTL), overvoltage- and overcurrent-protection, fixed frequency (500 KHz) conversion, and synchronization input. CB150D's operating temperature is -55 °C to +100 °C.

www.martekpower.com

MARTEK POWER

28 V input VME power supply

The VME28M is a MIL-STD-704A-F and MIL-STD-1275A compliant 28 V power supply for avionics and vetronics. It is a wide-input, ANSI VME64 and IEEE 1101.2-1998 compliant version for performance-driven utilization. Designed to satisfy many of today's military applications, the VME28M is available in 6U x 160 mm single-slot conduction-cooled or two-slot convection-cooled configurations. Rated for up to 250 W, output voltages of 3.3, 5.0, and ±12 VDC are provided. All of the power supplies meet MIL-STD-461 EMI, MIL-STD-810F environmental, and MIL-STD-901C shock requirements.

www.rantec.com

RANTEC POWER SYSTEMS, INC.

Direct spray enclosures offer flexible electronics deployment on airborne platforms

By Andy Finch

Photo courtesy of Northrop Grumman

Vehicle integrators are challenged to provide enhanced processing capabilities in unpressurized space on airborne platforms. Direct spray enclosures offer an alternative approach to environmentally isolate electronics in harsh environments to satisfy payload trends, reduce development time, and manage the entire technology life cycle.

Increasing demand for processing on manned or Unmanned Aerial Vehicle (UAV) platforms continually exceeds pressurized space for electronics. Movement of sensitive electronics to unconditioned compartments requires environmental isolation that many platforms cannot provide. Few solutions address the need for cost-effective flexibility in electronics selection and integration in harsh environments. Innovative packaging approaches, such as those utilizing direct spray, provide essential environmental isolation with the ability to mix commercial-grade air-cooled and rugged conduction-cooled electronics in the same enclosure. Besides successfully satisfying today's payload trends, direct spray enclosures offer reduced development time and life-cycle cost benefits.

Satisfying payload trends

More than ever, integrators are asked to provide more capability with less Size, Weight, and Power (SWaP), producing power densities in harsh environments that tax traditional cooling capabilities. Intelligence, Surveillance, and Reconnaissance (ISR) applications today relay critical information from the sensor on an airborne platform to the ground for compilation. Trends to reduce dependence on limited data link rates require more computing in the air. Parallel processing, floating and fixed point calculations, and filtering are common tasks performed in payloads such as radar and image processing, electronic warfare, signal processing, command and control, and mission processing. The ability to configure dedicated hardware with task-specific software using FPGA and DSP products for a wide variety of applications is attractive to leading vehicle integrators.

Unfortunately, such electronics consume 100-200 W per 6U slot (especially VPX), quickly exceeding air- and conduction-cooled enclosure and platform cooling capacity. As technology refresh cycles of avionics range from 8 to 10 years and processing electronics vary from 5 to 8 years, it is inevitable that some electronics will be forced out of conditioned space. Similarly, the growing demand for unpressurized UAVs places an equal burden on integrators to either ruggedize electronics or otherwise isolate more temperature-sensitive electronics, such as RF cards, from environmental extremes.

Ruggedizing electronics to relocate from stationary ground environments or pressurized compartments to unconditioned space with requirements ranging in altitude from 25,000 to 70,000 feet and temperatures from -65 °C to +71 °C has a significant effect on development schedules. Redesigning, manufacturing, and testing air-cooled boards for conduction cooling can take up to 12 months when industrial-grade component lead times alone exceed 6 months. If rugged air-cooled cards are used, compensation on RF cards is often required due to variations in temperature between first and last cards in the enclosure. Either way, extended development and integration timelines negatively impact the ability to quickly deploy payloads in harsh environments. Furthermore, every platform has different levels of cooling infrastructure, complicating integration when boards only exist in either air- or conduction-cooled configurations, but not both.

Adding functionality and performance unavailable when the electronic subsystems were originally deployed requires upfront planning to limit refresh costs to electronics, I/O, and software applications. Conduction- and air-cooled enclosures strain to deliver adequate cooling at extreme environments for today's electronics. As technology changes over the next decade, the probability that integrators can use today's enclosures without redesign for tomorrow's electronics is low. When systems are deployed without provision for growth in the form of per-slot cooling, overall heat rejection, or Environmental Control System (ECS) capacity, the cost of technology upgrades becomes significant. Another significant contributor to life-cycle costs is the electronics: Conduction-cooled electronics are typically twice the cost of their commercial-grade, air-cooled equivalents. Direct spray solutions ensure thermal headroom for future upgrades while enabling the flexibility today to deploy any electronics for use in harsh military environments.

Reducing development time

Air- and conduction-cooled cards are readily installed in direct spray enclosures for integration, testing, and production on military platforms. Aircraft such as RQ-4 Global Hawk (see photo courtesy of Northrop Grumman, first page of article), U-2 Dragon Lady, MQ-1 Predator, and MQ-9 Reaper are taking advantage of the inherent ability to use commercial-grade electronics in extreme environments, by using direct spray enclosures. In all cases, the electronics are located in unpressurized compartments on platforms with operational requirements as shown in Table 1. Even under such extremes, sensitive RF electronics can be heated and cooled with the ability to minimize temperature gradients to less than 2 °C for a 20-slot enclosure while boards range in power from 20 to 100 W/slot, obviating the need for temperature compensation. For air-cooled enclosures, gradients can be as large as 20 °C from the first to last slot.

Direct spray enclosures take about six months to configure I/O, identify and procure the desired backplane, and test the subassembly prior to customer electronics installation. During enclosure configuration, electronics hardware and software integration is possible in lab environments by mixing commercial-grade air- and/or conduction-cooled boards. Those same lab assets can then

Platform Requirements			
Temperature (°C)	-65 to +71		
Altitude (ft)	25,000-70,000		
Temperature Gradients	**Air**	**Conduction**	**Direct Spray**
ΔT°C ($T_{slot\ n}$ - $T_{slot\ 1}$)	20	10	2
Electronics (6U)			
Available Power Density (W/slot)	200	100	Either
GPP Cost	$8,000	$15,000	Either
FPGA Cost	$30,000	$40,000	Either
Lead Time (weeks)	8-16	26-34	Either
Enclosure			
Available Cooling Capacity (W/slot)	100	100[1]	500
Cost	$15,000	$25,000	$45,000
Projected Enclosure Capability			
Cooling Capacity (W/slot)	200[2]	200[3]	850-1,000

[1] Industry data for conduction. Few applications achieve this power density.
[2] Industry data for Air Flow Through (AFT) boards and enclosure
[3] Industry data for Liquid Cold Plate with conduction enclosure and boards

Table 1

be integrated on the platform for further qualification and deployment. Figure 1 depicts the timeline for electronics integration when ruggedization is required relative to commercial-grade electronics in a direct spray enclosure.

Managing life-cycle costs

General Purpose Processing (GPP) remains a necessary function in deployed enclosures by providing the user interface, system monitoring, and data acquisition running on operating systems such as XP, VXWorks, or Linux and analyzing the data preprocessed by DSP or FPGA boards. Commercial-grade GPP SBCs range from $5,000 to $10,000 per 6U card, while rugged conduction-cooled configurations average $15,000. When FPGA boards are available in air- and conduction-cooled versions, the percentage difference is smaller at $30,000 and $40,000, respectively. Table 2 represents the board cost differential for an integrated enclosure on a per-slot basis.

Direct spray enclosures with cooling system components cost about $20,000 more than equivalent conduction enclosures and approximately $30,000 more than air-cooled enclosures in quantities of less than 10 (see again Table 1). In the case of a direct spray, this includes the cooling system, card cage housing the

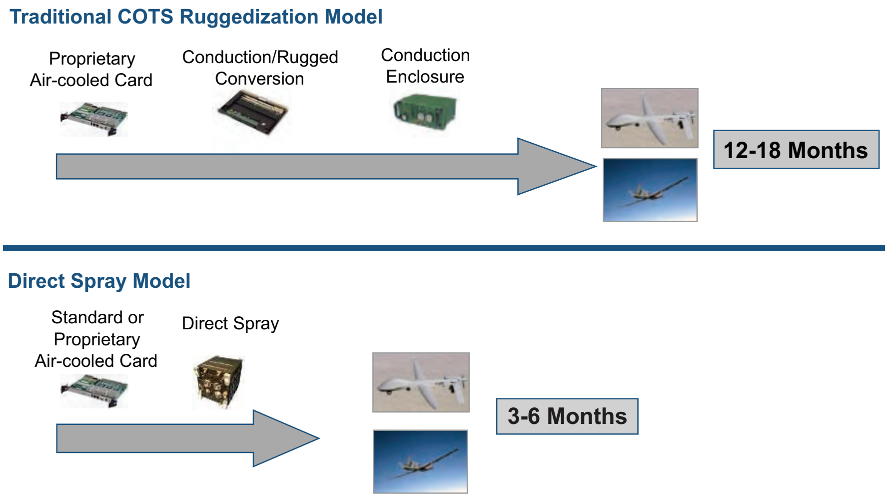


Figure 1

Slot Count	GPP – Air	GPP – Conduction	Cost Difference
4	$32,000	$60,000	$28,000
5	$40,000	$75,000	$35,000
6	$48,000	$90,000	$42,000
7	$56,000	$105,000	$49,000
8	$64,000	$120,000	$56,000
9	$72,000	$135,000	$63,000
10	$80,000	$150,000	$70,000

Slot Count	FPGA/DSP – Air	FPGA/DSP – Conduction	Cost Difference
4	$120,000	$160,000	$40,000
5	$150,000	$200,000	$50,000
6	$180,000	$240,000	$60,000
7	$210,000	$280,000	$70,000
8	$240,000	$320,000	$80,000
9	$270,000	$360,000	$90,000
10	$300,000	$400,000	$100,000

Table 2

“For larger airborne enclosures housing 5 to 20 slots, the cost savings in electronics can be five times the added expense of the direct spray enclosure and cooling system.”

electronics, and enclosure as shown in Figure 2. For air- and conduction-cooled enclosures, the requisite platform-level cooling hardware is not included in the costs presented. The enclosure cost differential between direct spray and conduction is easily overcome when three or four of the boards are air- versus conduction-cooled.

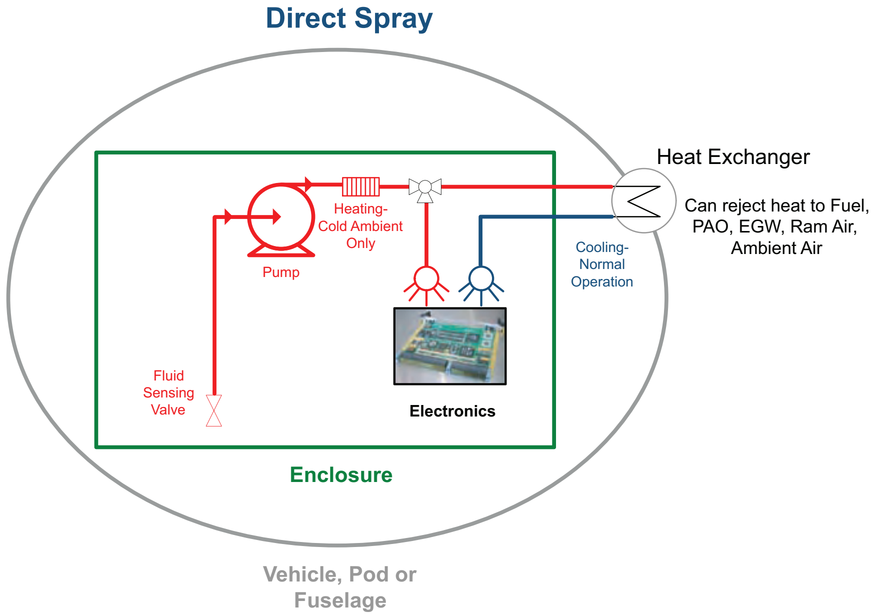


Figure 2

For larger airborne enclosures housing 5 to 20 slots, the cost savings in electronics can be five times the added expense of the direct spray enclosure and cooling system. Costs throughout the life cycle are deemed important, as airborne platforms are expected to have a 30 to 40 year useful life. For KC-135s and B-52s, the reality is greater than 60 years of deployment because the economics of upgrades and refurbishment outweigh the development costs of new planes. Incremental technology refresh cycles are common on today's aging aircraft. Direct spray systems confine refresh costs to purchasing next-generation electronics, configuring I/O, developing software, and tuning the card cage spray for different boards. This is made possible by the inherent thermal headroom of direct spray enclosures.

Direct spray enclosures enable any electronics to be upgraded over multiple refresh cycles with proven power densities of 500 W per slot on demonstration boards and industry projections of 850-1,000 W per slot per 6U card. As the overall heat load of a direct spray enclosure increases, a heat exchanger (see again Figure 2) mounted in the aircraft can be scaled to meet the payload requirements. The thermal headroom offered by direct spray enclosures in the foreseeable future provides integrators development and upgrade cost savings. When systems are deployed with provision for growth in the form of per-slot cooling capability and overall heat rejection, the cost of technology upgrades is reduced over the aircraft life cycle.

Direct spray: Meeting modern demands

Direct spray enclosures support the trend for more processing payloads co-located with the sensors on air platforms, especially for unpressurized, SWaP-constrained UAVs. Subsystem integration time and cost reductions arise from the ability to readily accept air-cooled, conduction-cooled, and custom boards. Because the enclosure and heat exchanger constitute an autonomous subsystem without dependence on cooling infrastructure such as an ECS, platform-level integration is simplified. The ability to integrate and deploy commercial-grade electronics in extreme environments affords procurement lead time advantages and cost savings. Direct spray enclosures, like those produced by SprayCool, also enable development time and production cost savings. With intrinsic thermal headroom, the cost savings extend over the platform life cycle.

Andy Finch *is product manager for SprayCool where his responsibilities include product roadmaps, product positioning, partnership development, and market research. Since joining SprayCool in 2000, he has held engineering and management positions supporting program management, product development, and systems engineering. Prior to SprayCool, he developed control systems and automated equipment for the food processing, agricultural, and HVAC industries. Andy earned a BSME from the University of Idaho, an MS in Engineering from Purdue University, and an MBA from Indiana University. He can be contacted at afinch@spraycool.com.*

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U.S. Air Force photo by Staff Sgt. Shawn Weismiller

Structured ASICs: A clear advantage when designing advanced military and aerospace electronics

By Barry West

Today's military and aerospace electronics face challenging environments as well as increased security and production handling requirements, and must adhere to stringent reliability specifications while fitting an effective business model. Three custom logic options exist – FPGAs, traditional cell-based ASICs, and structured ASICs. But structured ASICs offer clear advantages over their competition.

The advanced capabilities of military and aerospace electronics available today can be clearly seen in the improved performance, efficiency, and safety of new commercial aircraft. These capabilities have changed the way soldiers fight the war against terrorism. A primary contributor to the advancement of these next-generation applications is the complexity of the electronic systems used to design these leading-edge and increasingly autonomous systems. Just like the designers of consumer or telecommunications electronics, mil/aero product designers need access to advanced deep-submicron process technologies to meet the specifications of future products. In addition, they need access to complex IP such as microprocessors and DSP cores, as well as high-performance memory and serial interfaces.

Mil/aero designs often have special requirements that make them more difficult than commercial applications, posing unique problems to system designers. Challenging environmental conditions, enhanced security and production handling requirements, and stringent reliability specifications contribute to the complexity of design and limit the choices of which technologies and IP can be used. Additionally, mil/aero electronics are difficult to fit into an acceptable business model as they are usually low-volume applications, making it difficult to justify very expensive technology tooling costs for cutting-edge process technologies and large licensing fees for advanced IP.

There are three options for a systems designer who needs to implement custom logic in a mil/aero electronic application: FPGAs, traditional cell-based ASICs, and structured ASICs. We'll review each option and detail why structured ASICs offer clear advantages over the others (Table 1).

Are FPGAs a fit for mil/aero applications?

At first glance, FPGAs appear to have compelling advantages for logic solutions in mil/aero applications. The latest generations of these programmable devices offer impressive performance capabilities and come with an extensive library of embedded and soft IP functions. Advanced IP like microprocessors and memory interfaces available in these devices make them attractive for avionics applications. The advanced IP and in-system reconfigurable logic seem like an ideal match for Software-Defined Radio (SDR)-based communication systems, which need high performance and the ability to change hardware configurations during operation.

These capabilities also add value in many different military applications such as smart munitions, cryptography, and battlefield electronics such as night vision goggles. FPGAs can be bought in limited quantities and don't have non-recurring engineering charges, which contributes to reduced product and development costs. All of these factors are important to mil/aero system providers. However, when

Mil/Aero Application Requirement	Special Considerations	FPGA Solution	Cell Based ASIC	Structured ASIC
Security	Reverse Engineering, Tampering, Obfuscation	Poor Bit Stream Vulnerable Bit Stream Encryption	Good Non Volatile Metalized Difficult to Rev Engineer or Modify	Good Non Volatile Metalized Difficult to Rev Engineer or Modify
Airborne Radiation Resistance	Flight Critical Avionics	Very Poor Configuration Stored in SEU Vulnerable RAM based LUTs	Good Pre Defined Logic ECC/Redundancy to Enhance	Good Pre Defined Logic ECC/Redundancy to Enhance
Power	Battery Applications Small Form Factor	High Power Inefficient Logic Arch Unused Logic Powered	Lowest Power Most Efficient Logic Arch No Unused Logic	Low Power Efficient Logic Structure Unused Logic not Powered
Special Handling	ITAR, On Shore, NOFORN, Trusted	Limited Nearly all FPGAs are Non Compliant	Yes Options Available for Design Through Prod Support	Yes Options Available for Design Through Prod Support
Development Time to Market	Qualification Requirements	Short Pre Verified IP Hardware Available Quickly No Manuf of Prototypes	Long Complex IP Integration Complex Development Cycle Full Manuf Span to Protos	Medium Pre Verified IP Medium Development Cycle Partial Manuf Span to Protos
Development Cost	Low Cost of Entry	Low Development Cost No Tooling Low IP Cost	High Development Cost Expensive Tooling High IP Costs	Medium Development Cost Minimized Tooling Reduced IP Cost
Respin Cost	Version Updates, Bug Fixes	Very Low Firmware Update Changes Hardware	Very High Expensive Mask Costs Difficult ECO Flow	Low Limited Number of Prog Levels Simple ECO Flow
Production Cost	Low/Medium Vol Mil/Aero Programs	Low Vol Support Very High ASP	Very Expensive in Low/Medium Vol High Vol Required for Low ASP	Medium to Low ASP Low to Medium Vol

Table 1

looking deeper into additional requirements of mil/aero applications, the match between these systems and FPGAs is not as good as it might initially appear.

In avionics applications for both the commercial and military sectors, flight-critical electronic devices are exposed to higher levels of neutron radiation, which can cause Single Event Upset (SEU) issues on small process geometry RAM elements. These, in turn, typically cause a temporary stored data loss in a memory device. This effect is of particular concern in SRAM-LUT-based FPGAs, where logic configuration data is stored in RAM elements. Configuration data upset in the RAM-based LUT can potentially result in a device-level logic error. This phenomenon has been a well-known consideration in avionics applications for more than a decade. FPGAs also require from 500 ms to 800 ms at power-up to facilitate programming a mid-sized advanced FPGA into its functional configuration. This can cause concerns in the case of system power-down or reboot during flight. These issues make SRAM-based FPGAs a very poor, and in many cases, forbidden, match for flight-critical applications.

A military radio based on SDR electronic systems needs to be carried into battle and function for many hours or days on battery power. This means these systems must be as light as possible and be very efficient for dynamic and leakage power consumption. Even though FPGAs meet the need of configurable logic and advanced IP for these devices, they also consume large amounts of static and dynamic current because of their LUT-based logic structure. The ability to have fully reprogrammable logic means inefficient structures that draw a lot of power during operation. The complex FPGAs used in these applications can consume 6 W of power or more in cases where large amounts of logic are used and high performance is required.

Certainly, a degree of in-system reconfigurable logic is required to implement goals of dynamic waveform generation, but the degree to which FPGAs are relied upon in current radio architectures drives current radio designs well out of acceptable ranges for power budget and form factor requirements. Again, the special requirements of these systems make complex FPGAs a poor fit in meeting the full operational requirements of the system. This is true for all battery-operated devices including night vision goggles, as well as other communication systems.

Security is also a factor in all military applications, and FPGAs are inherently susceptible to security intrusion because they require off-chip ROM or processor loading to store the logic configuration bit-stream information. Despite advances in encryption techniques, this data is still easily compromised by hostile forces and can be used to build equivalent hardware with little difficulty. Military applications also require special manufacturing handling such as ITAR support and/or NOFORN processing in U.S.-based manufacturing facilities. Nearly all of today's advanced FPGAs cannot support these requirements, as they are built outside of the United States in facilities that do not support special handling procedures. These factors limit the acceptability of FPGAs in mil/aero applications based on required standards of device security and assured production access, making them a non-ideal solution.

Expensive cell-based ASICs are difficult to justify

Cell-based ASICs solve many of the issues involved when using FPGAs. They can be designed for very low power and, by the nature of nonvolatile logic, have enhanced security and are live at power-up. There is also a wide variety of IP types available from many different vendors, supported at a variety of foundries. The best power, performance, and IP availability make cell-based ASICs an attractive technical option.

The associated trade-off with these semi-custom devices is that they are less cost effective for low- to mid-volume mil/aero applications requiring technologies more advanced than 130 nm. The cost to develop a custom 90 nm ASIC can range from $2 to $5 million when considering the high tooling costs, IP licensing and usage charges, and engineering development cost. It takes a significant amount of engineering resource to create and verify a design in 90 nm technology when typical complexity can include millions of gates of logic, several complex IP blocks, millions of bits of memory, and 500-plus I/O. It is not uncommon for a team of five to eight engineers to need more than a year to achieve tape out on a design of this complexity. And if anything is missed during verification causing silicon failure – or if features need to be adjusted or added during prototype evaluation – then the schedules are delayed even more and the costs continue to mount.

For mil/aero applications, cell-based ASICs using technologies 130 nm and larger can be a good fit. For 90 nm technologies and below, increasingly few military or aerospace programs can justify the expense and lead time required to develop cell-based ASICs for applications that will run in production volumes on the order of 50K units a year or less.

Structured ASICs meet the special needs of mil/aero applications

The structured ASIC was created to specifically address FPGA and traditional ASIC shortcomings and offers compelling advantages for system designers when compared to FPGAs and cell-based ASICs. Structured ASIC platforms also allow designers to have access to advanced technology nodes that offer the performance and IP portfolios needed for today's sophisticated mil/aero applications just like FPGAs and cell-based ASICs. But compared to FPGAs, the structured ASIC can be produced at mid to low volumes at significantly lower production costs. And compared to cell-based ASICs, the structured ASIC has much lower development costs because it shares tooling and IP licensing expenses across many devices and offers an optimized development span. This makes it a better fit for mid- to low-volume production.

The traditional fit of structured ASICs in the market is clearly shown in Figure 1, which includes the relative cost and span for each option. But beyond these traditional benefits, structured ASICs also solve many of the mil/aero system issues described in the previous sections. Consider the following military and aerospace applications and how a structured ASIC could meet the requirements for each.

For battlefield communication applications such as a Joint Tactical Radio System

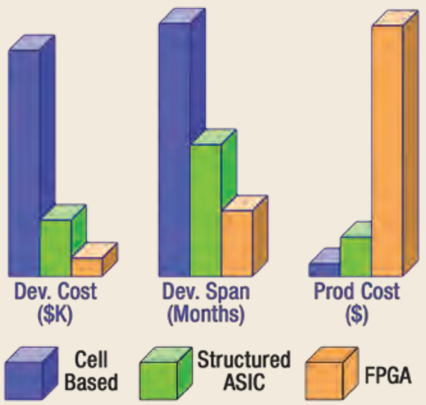

Figure 1

(JTRS)-based SDR or any portable military device that will depend on battery power, a structured ASIC can be an effective fit. A structured ASIC platform that supports processing elements for General Purpose Processing (GPP) and DSP requirements – as well as significant quantities of custom logic combined with standard interfaces such as DDR, LVDS, and Ethernet – is a good fit for these systems.

Consider the block diagram in Figure 2, which shows an SDR system architected using a large structured ASIC that can handle the high-performance algorithms common across all JTRS waveforms, combined with a smaller FPGA to handle the reconfigurable needs of these systems. An architecture such as this can use up to 10x less power than a system built out of multiple large FPGAs, which is common in the current generation of SDR systems. This is because the structured ASIC architecture uses ASIC-like logic structures and libraries that are significantly more power efficient than FPGA LUT-based logic while still giving high performance. Smaller devices, much lower power, and a greater degree of physical security all lead to a system more in line with form-fit-function program objectives.

For an application that has cryptography requirements or other security concerns (such as military communications) or any application that could be a target for enemy tampering, a structured ASIC can be an effective solution. The structured ASIC does not need a discrete device to provide a bit stream that is required to program an FPGA device. A bit stream is relatively simple to tamper with and decipher, and once hostile forces have it, they can program equivalent devices with little difficulty. If a structured ASIC also contains an embedded battery-backed memory device such as Security Enhanced XPressArray (S-XPA) from ON Semiconductor (formerly AMI Semiconductor), then cryptography and anti-tamper IP such as AES encryption engines or secure key processors can be added to a system with the keys stored in a secure on-chip memory. This increases security levels and makes hostile tampering or reverse engineering more difficult in any sensitive military application.

In the case of avionic electronics such as flight-critical control applications, a

SDR Architecture with Structured ASIC

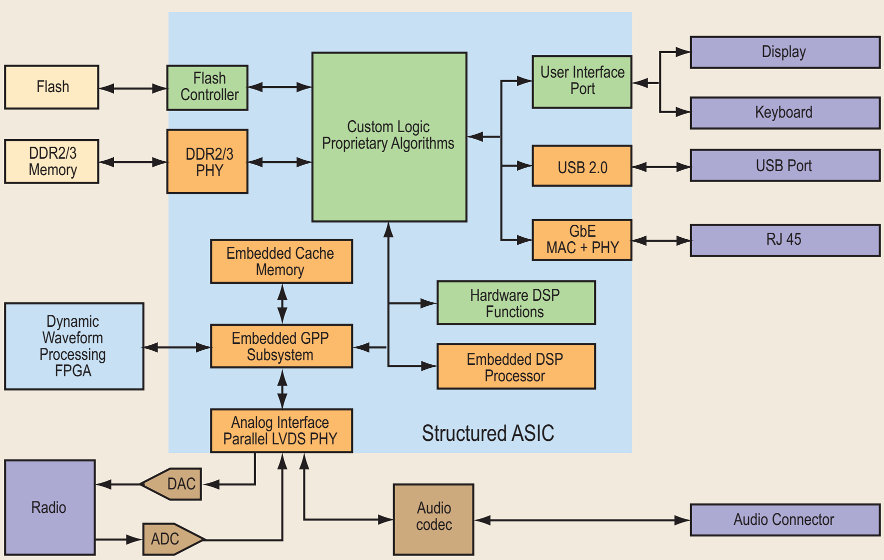

Figure 2

structured ASIC can meet the requirements of systems where dependable operation is crucial. Access to a cost-effective solution that provides high performance and advanced IP but also meets reliability requirements for SEU performance and live on power-up technology gives the aerospace electronics designer a significant advantage. The structured ASIC platform can support IP such as microprocessors, standard interfaces such as PCI and Ethernet, and error detection and correction algorithms while providing for plenty of RAM and custom logic to implement any proprietary functions needed for these applications. Combine that with high reliability and low cost and you get a solution that is ideally suited for these applications.

Specific to the types of low-volume and low-cost applications predominant in the military and aerospace industry, the structured ASIC is a much better overall solution when compared to a cell-based ASIC. Structured ASICs have lower hardware costs because only a few custom masks are needed to program the base-level silicon into the specific device. And even though the design flow for a structured ASIC is similar to a custom ASIC flow, it can be more efficient by relying on pre-verified and embedded IP that is already qualified and proven in the technology being used. Devices like the XPressArray family from ON Semiconductor are manufactured in the United States and support full on-shore design, manufacturing, assembly, and test flows to meet special handling requirements for sensitive military electronics.

The most benefits for military systems

The benefits of structured ASICs for military and aerospace systems are growing increasingly clear. They go beyond the immediately tangible power and cost benefits compared to FPGAs and the development cost of custom ASICs to include more specific benefits of enhanced security, improved reliability in harsh operating environments, and the ability to meet the "trusted" manufacturing requirements of military applications. Accordingly, using structured ASICs that allow for on-shore manufacturing and include the required IP enables suppliers of military and aerospace electronics to build applications that meet the special requirements of this market.

Barry West *is principal systems architect, mil/aero and digital products/services at ON Semiconductor. He is responsible for working with customers to define system architectures to meet their system requirements and for defining product roadmaps for mil/aero applications. Additionally, he is an expert in many EDA design tools including synthesis, STA, and physical design and verification. He can be reached at Barry.west@onsemi.com.*

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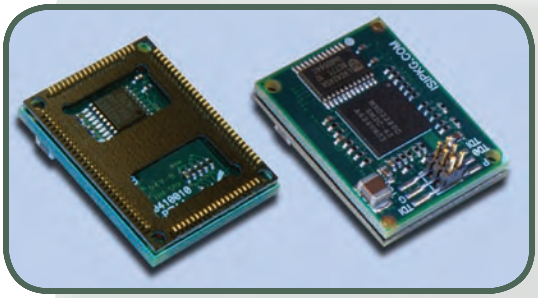

Adapters for obsolete SMT devices

The joke is that some COTS electronics go obsolete with the changing Christmas buying seasons, making it very difficult for mil programs to stock some surface-mount technology ICs over a 10-year period. However, Interconnect Systems Inc. is aiming to thwart the obsolescence Grinch via their footprint-conversion-enabling FlexFrame adapters. FlexFrame is designed to replace oft-obsolete j-lead and SMT gullwing IC packages such as PLCCs, QFPs, SOICs, and TSOPs.

Called "FlexFrame" because of its flexible configuration, the adapter includes several standoff heights, "unique" pitch and pin location, and carrier windows allowing center-of-interconnect component placement. The high availability FlexFrame design accomplishes its mission via PhosBronze pins tucked inside an FR4 carrier, then shaped to mimic the j-leads or gullwing. A reliable, rugged interconnect is then formed once FlexFrame's connector gets soldered between the host PCB and the adapter. Now, if only FlexFrame could just keep this Christmas's stash of electronic gadgets from going obsolete!

Interconnect Systems Inc. • www.isipkg.com • RSC# 39416

LynxOS RTOS now runs on Core 2 Duo

All that desktop multicore goodness was bound to make some mil designers want to cozy up to some determinism in the form of a good, old-fashioned RTOS. So Curtiss-Wright Controls Embedded Computing (CWCEC) [will we ever stop chuckling at the length of that company name?] broke down and ported LynxOS SE 5.0 to its 6U VME SVME/DMV 1901 Intel-based SBC. Since not all RTOSs are created equal, it's important to note the POSIX-conformant RTOS is also the basis for LynuxWorks' efforts with MILS and separation kernels.

Now appearing on a SVME/DMV 1901 near you, the LynxOS SE 5.0 RTOS Board Support Package (BSP) provides a Linux-binary compatible OS to enable faster mission-critical application development. LynxOS SE 5.0 also provides "medium assurance security" as afforded by the single-level OS protection profile. In addition, the system offers an enhanced Linux ABI and an updated GNU tool chain for a streamlined execution and design environment. Meanwhile, the rugged SVME/DMV 1901's Core 2 Duo and VME64x air-cooled design supports a wide range of front panel I/O, including SCSI and video graphics, while rear I/O configurations lend support to optional dual video display.

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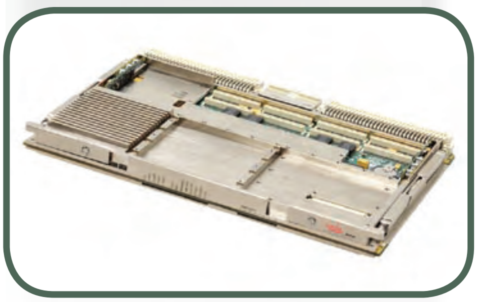


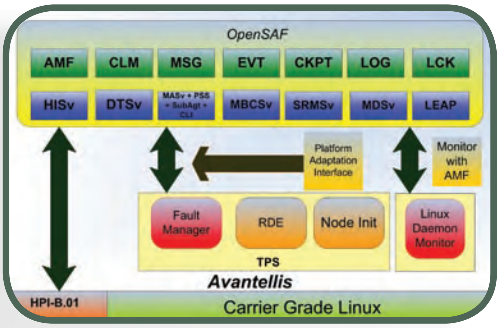
250 MHz, four 12-bit channels

We've said it before, and we'll keep on saying it: The real world is *analog* – this digital stuff is just a way to manipulate the data. But to do that, it's essential to convert as much high-resolution analog data into the digital domain. To do that requires lots of channels and as many bits as one can cram on a card. Enter GE Fanuc's ICS-1650 high-speed ADC, delivering simultaneous sampling rates up to 250 MHz on four 12-bit analog channels.

Ideal for SDR, SIGINT, radar, and diagnostic imaging apps, the Virtex-5 powered analog-to-digital converter provides a four-lane PCI Express bus interface delivering a net payload data rate as fast as 1.25 GBps. Not only that, ICS-1650 affords a continuous data acquisition sampling speed on all four channels in excess of 200 MHz, while providing SFFs (and particularly microATX) with mechanical compatibility. Additionally, users needing help with sometimes-tricky FPGA code development can turn to the ICS-1650's Hardware Development Kit, which includes timing constraints, VHDL source code, ISE projects, and Test Bench. An optional Graychip GC5016 ASIC can be added for more DDC functionality. Then there's the 16 MB QDR II SRAM provided for "scratchpad" use – appropriate since we think the ICS-1650 is something to write home about.

GE Fanuc Intelligent Platforms • RSC# 38089 • www.gefanuc.com

No middle-of-the-road availability for *this* middleware



Those who want 100 percent perfection are typically said to have "unrealistic expectations," but it appears that Emerson Network Power is aiming to come pretty darn close with its High Availability (HA) Avantellis middleware. Avantellis is geared toward industrial and military apps requiring "greater than 5NINES availability," Emerson reports. With the final .001 looming somewhere in the equation, Avantellis middleware is the first commercially available incarnation of the Service Availability Forum's (SA Forum's) OpenSAF open source code base.

As with most middleware, resigning Avantellis to just one application or system would be nearly impossible because of its inherent adaptability to many OSs, processors, and hardware platforms. The portable, modular Avantellis, which utilizes the SA Forum's Hardware Platform Interface (HPI), also complies with the SA Forum's Application Interface Specification (AIS). AIS provides an Availability Management Framework to coordinate a distributed computing environment's redundant resources without any one point of failure, and monitors component status inside the cluster. Also offered is the LCK/GLSv distributed lock service, allowing shared resource access coordination on multinode applications. And finally, one more notable among myriad others is the Checkpoint Service (CKPT/CPSv), which affords a facility where checkpoint data can be recorded incrementally and retrieved after switchover or failover; then execution can commence once again in a correct state.

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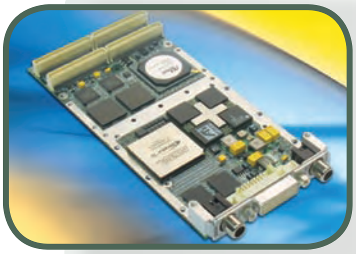
 – *Continued from page 43*



Two heads really are better than one

Some of our lucky editors have dual independent displays on their desk, greatly enhancing productivity. So why not do the same with your rugged, deployed defense system? Now Aitech is proving that this type of uber-productivity can be implemented in modern military apps via its M590 multi-standard video and graphics PMC featuring dual independent graphics heads. The hale and hearty PMC is compliant with PCI-X Rev 1.0b and PCI Rev. 2.3 and delivers output from two individual data streams, sending the data to two separate monitors. Video and imaging input streams can also be separated by an onboard FPGA.

M590 – ideal for tactical area moving map applications, advanced sensor fusion, and more – provides 2D and 3D image capture/frame grabbing and video display. It also offers underlay and overlay with resolutions up to 1,536 x 2,048 at refresh rates of 30 to 200 Hz and 32 bits per pixel (Truecolor+) for high-res man-machine interfaces. The 2D and 3D video operations can be unified in several parallel pipelines while preventing internal and external data path overloads. Some of M590's other features worth a double take include: progressive RGBHV/RGsB; LVDS single/double link; composite/S-video supporting NTSC, PAL, and RS-170; external or internal sync; and support of advanced non-interlaced or interlaced monitors. M590 is available in air- or conduction-cooled versions and includes ALT Software's OpenGL 2D and 3D VxWorks and INTEGRITY drivers.

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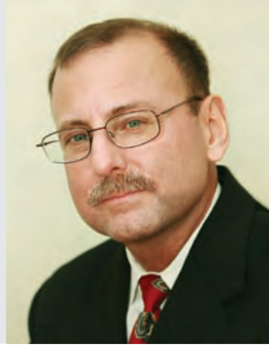
SSDs on solid ground ... and in the air



By Chris A. Ciufo, Editor

Nonvolatile storage has long been a part of military equipment. After all, bubble memory was available from guys like Intel, Texas Instruments, Allen Bradley, Thomson, and others for a long time. But magnetic bubble memory was last used in *legacy* military systems before it became really-truly-honestly-no-foolin' obsolete in the late 1980s. Today, anyone with a new cell phone or digital camera knows just how cheap nonvolatile flash storage has become. That same technology is finding its way into solid-state disks, on boards, and into modern deployed defense systems. Bundle a bunch of flash devices together with a controller and some logic and you've got a solid-state disk. Cheaper is not always better, and not all nonvolatile storage is suitable for disk duty.

It's important to define what an SSD is. The strictest definition is nonvolatile storage in either 2.5-inch (laptop) or 3.5-inch (desktop) form factors with COTS interfaces such as EIDE or SATA/SATA II. In this configuration, vendors such as InnoDisk, PQI, Seagate, Super Talent, or SiliconSystems package NAND flash, a controller, interface, and wear-leveling logic into the familiar disk drive package[1]. The devices *look* identical to regular magnetic rotating drives (HDDs), may consume less power, are dramatically faster, are really rugged (no moving parts), and often have hardware security features such as scrubbing and encryption. SanDisk FFD SSDs, for example, feature secure erase and sanitize – two features that remove data, overwrite it, and assure that no trapped charge (1s and 0s) remains. The company's *autoresume* feature guarantees the process completes if a power cycle or other anomaly occurs. This is handy in vetronics and airborne systems where "dirty" power is all too common.

The beauty of packaging microprocessors and FPGAs into SSDs is that erasure or data striping algorithms and custom interfaces can be created. Imagine an SSD that bolts up to ARINC-429. At the 2008 *CMSE* conference, SiliconSystems described the impending obsolescence of parallel ATA chipsets and posited an FPGA replacement that could speed data transfer via built-in DMA and signal rise/fall/propagation shaping. As well, a host-based proprietary security algorithm can interact with a custom interface and on-chip logic to provide NSA-quality data encryption. None of these things are possible with a plain old magnetic HDD, nor with limited capacity consumer-quality SD/MicroSD digital camera cards.

Whereas consumer flash is limited to about 32 GB in SDHC with a street price of under $150, SSD densities continue to increase as NAND flash prices fall precipitously[2]. As we went to press, SiliconSystems announced their SiliconDrive II series SATA in 2.5-inch size at 64 GB with full wear-leveling, ruggedization, and data protection. Weeks before, Super Talent – a relatively new name in COTS military circles – was selling their commercial temp *MasterDrive* 128 GB SATA II, 2.5-inch SSD at a street price around $300. The company's rugged DuraDrives cost more, but commodity-like price wars bode well for military designers and their end systems.

But not all SSDs are strictly flash-based. Texas Memory Systems recently announced a patent on their Instant-On I/O (IO^2) RamSan products that use DRAM for fast, dense storage and triple-redundant internal UPS to protect against power loss. Where flash-based SSDs have sustained read/write times on the order of magnetic HDDs (approximately 40 MBps), DRAM-based SSDs are in the InfiniBand and Fibre Channel range of 3 GBps. At the other end of the spectrum are chip-based nvSRAMs from companies like Simtek (recently acquired by Cypress Semiconductor) whose 8 Mb devices achieve 25 ns READ access by bolting SRAM and EEPROM cells together.

Another unique SSD chip-level technology comes from Freescale and their partner e2v (formerly Thomson TCS, France). Designed from the get-go for high-rel markets like automotive, industrial, and military, Magnetoresistive RAM (MRAM) stores data based upon *electron spin* instead of trapped charges or active power-burning transistors. The devices offer the speed of SRAM, the density of DRAM, the nonvolatility of flash, and with minimal modifications are operable in radiation environments such as space. e2v just launched a mil-grade 4 Mb device to market, with promises of higher future densities. Extraordinary speed and simple endurance – without necessitating complex wear-leveling logic – have a definite place in defense systems. In short, an MRAM might be the best way of all to construct future SSDs.

Still, Multi-Level Cell (MLC) 2-bit NAND flash ICs remain the mainstay of the SSD market because they're available in mega*byte* chip densities. Issues of wear-out endurance and secure erasure have been solved at the drive level. There are future promises of 3- and 4-bit cell devices from Intel-Micron, Numonyx/Hynix, Samsung, and SanDisk/Toshiba that promise densities from 512 Mb to a staggering 64 Gb[3]. At Intel's recent IDF conference, the company announced a series of flash-based SSDs and storage blades promising an order of magnitude better endurance while dramatically reducing power using as-yet-unspecified proprietary magic. I'll dig into that further and pass on what I find.

Clearly the market for SSDs continues to *ahem!* grow larger all the time. No doubt ground-, airborne-, shipboard-, and even space-based military systems will continue to rely on solid-state over old-fashioned magnetic HDDs.

---

[1] Some SSD suppliers: SiliconSystems, Super Talent, Ridata, Seagate (yes, that Seagate), Intel, STEC, Texas Memory Systems, Adtron (recently acquired by SMART Modular Technologies), Simtek/Cypress Semiconductor, Micron, and Toshiba.
[2] Rule of thumb for pure consumer packaged flash: $1/GB. For consumer SSDs: $2-$4/GB. Rugged prices are easily 5-10x that, depending upon value-add features.
[3] "NAND Flash Memory Chip Size Trend," Report #F11201; July 2008. Forward Insights.